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# Timing Jitter Analysis for Clock Recovery Circuits Based on an Optoelectronic Phase-Locked Loop (OPLL)

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**Abstract:** Timing jitter of an OPLL based clock recovery is investigated. We demonstrate how loop gain, input and VCO signal jitter, loop filter bandwidth and a loop time delay influence jitter of the extracted clock signal.

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## 1. Introduction

In high-speed optical communication systems, operating at 160 Gb/s and above, the clock extraction may be performed using Optoelectronic Phase-Locked Loop (OPLL). The performance of the Clock Recovery (CR) circuit can be evaluated by measuring the temporal accuracy of the recovered clock signal (timing jitter). Timing jitter analysis of electrical PLLs is a subject of great importance and a large amount of literature is available on this topic, see e.g. [1]. Possibly, the most general and rigorous treatment is that of Mehrotra [2]. However, compared to the electrical PLL, the loop length of an OPLL is longer due to pulse compression stages or fiber amplifiers. A time delay must therefore be included into the analysis. In this paper, we extend the analysis presented in [2] by including a time delay in our model equations and thereby analyzing the particularly interesting case to OPLL. The combined effect of the input OTDM data signal jitter, the VCO signal jitter and the time delay, on the extracted clock signal jitter, is investigated by using the model. Furthermore, we compute the minimum obtainable timing jitter of the extracted clock signal.

## 2. Model set-up

The set-up of the balanced OPLL based CR, on which we base our model, is shown in Figure 1.

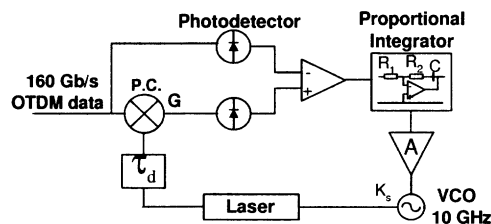


Fig. 1. Schematic set-up. Overall loop gain,  $\zeta$ , is defined as a product between: mixer gain (G), photodetector responsivity, (R), amplifier (A) and VCO, ( $K_s$ ).

The total accumulated time delay,  $\tau_d$ , is schematically indicated to occur between the optical clock generating laser and the phase comparator, (P.C.). The phase comparator mixes the optical OTDM data signal (e.g. 160 Gb/s) with the locally generated optical clock signal at the base rate (e.g. 10 GHz) producing an error signal. The mixing process corresponds to a mathematical multiplication with a mixer gain, G. In practice, non-linear processes like FWM in SOAs can be used to achieve the mixing, e.g. the experimental realization that this model is based on [3]. The error signal is sinusoidal with a frequency  $\Delta f$ , given by the difference between the 16<sup>th</sup> frequency component of the clock signal and the line rate of the data. The amplitude of the error signal is proportional to  $s_1 c_{16}$ , which is a harmonic product between the 1<sup>st</sup> and 16<sup>th</sup> Fourier frequency component of the corresponding data and clock signal. The balanced photodetection (BW 100 MHz) provides the subtraction of the DC level from the error signal, which results in a bipolar error signal. This subtraction also helps to stabilise the error signal against fluctuations in the input powers. The signal is then low pass filtered and fed back to the VCO, which controls the optical clock generating laser. The extracted clock signal will also contain phase noise which results in timing jitter due to the input OTDM data and VCO signal phase noise combined with noise from the loop components. For simplicity we only consider noise associated with the input OTDM data and the VCO signal. The phase noise of the input OTDM

data and VCO signal can be modeled as a Brownian motion phase error. In the presence of noisy signals we model the OPLL as an Ornstein-Uhlenbeck process as reported in [2].

### 3. Timing jitter as a function of loop gain

In this section, the impact of increasing overall loop gain on the extracted clock jitter is investigated. However, we first investigate how the spectrum of the extracted clock signal is affected by the input OTDM data and the VCO signal timing jitter.

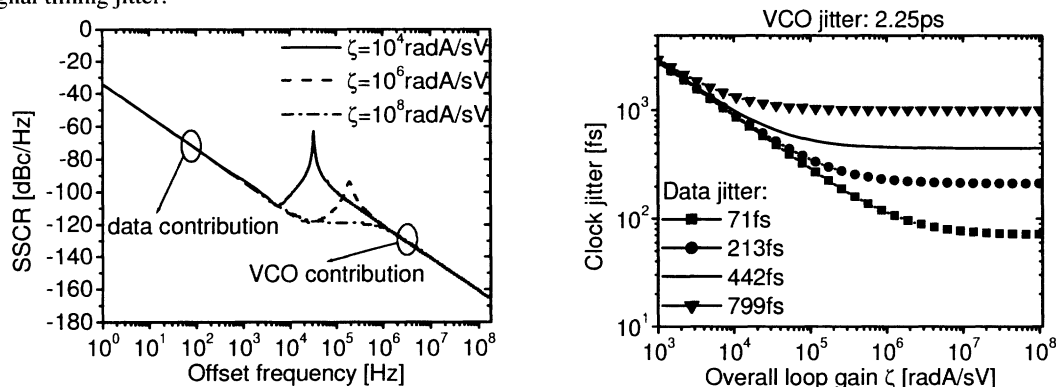


Fig. 2. (a) SSCR of the extracted clock signal for selected values of the overall loop gain. (b) Timing jitter of the clock signal as a function of the overall loop gain for selected values of input OTDM data signal timing jitter. VCO jitter is 2.25 ps and PI filter bandwidth is 20 MHz.

In Figure 2(a), Single-Side band to Carrier Ratio (SSCR) of the extracted 10 GHz clock signal, around the first harmonic (i.e. 10 GHz), is computed when the overall loop gain,  $\zeta$ , is varied from 10<sup>4</sup> radA/sV to 10<sup>8</sup> radA/sV. It is observed that the SSCR lays in-between two straight lines. These are contributions from the input OTDM data and VCO signal. Note that for low frequencies the clock SSCR follows the input OTDM data signal SSCR and for higher frequencies it follows SSCR of the VCO. The offset frequency, at which the SSCR of the clock signal starts to follow the SSCR of the VCO, corresponds to the bandwidth of the OPLL. This implies that the low frequency timing jitter is directly transferred from the input OTDM data signal to the clock signal, while the high frequency timing jitter of the clock signal originates from the VCO. In general, we are interested in reducing the high frequency jitter from the clock signal since it may result in a penalty when using the clock signal for optical gating. As the overall loop gain,  $\zeta$ , is increased from 10<sup>4</sup> radA/sV to 10<sup>8</sup> radA/sV, the SSCR of the clock signal becomes less and less influenced by the VCO signal. The sideband is pushed down and away. For sufficiently large values of the overall loop gain, the SSCR of the clock signal will approach the SSCR of the input OTDM data signal. This is also shown in Figure 2(b) where timing jitter of the extracted clock signal (jitter integration range: 1 Hz – 5 GHz) is plotted as a function of the overall loop gain,  $\zeta$ , for input OTDM data signal jitter in the range from 71 fs to 800 fs (jitter integration range: 1 Hz – 80 GHz). Increasing  $\zeta$  reduces timing jitter of the clock signal in general. As the overall loop gain is increased sufficiently, clock timing jitter approaches its minimum value. It is worth remarking that this minimum value corresponds to the input OTDM data signal jitter. However, when the input data signal jitter is relatively large, i.e. 800 fs, the minimum obtainable jitter of the clock signal is approximately 1 ps.

### 4. Timing jitter in the presence of time delay

The influence of time delay on the timing jitter of the extracted clock signal is investigated by looking at the SSCR of the extracted clock signal, Figure 3(a), for zero and 300 ns time delay. Having a loop time delay of 300 ns (loop length  $\approx$  60 m) is obtainable if having an EDFA in the loop. Notice that the SSCR of the extracted clock signal increases, around the resonant peak, when the time delay is 300 ns compared to the zero time delay case. This results in an increased timing jitter from 188 fs to 621 fs. In the presence of time delay, the behavior of the loop is very much dependent on the PI filter bandwidth [4]. We therefore need to investigate the timing jitter dependency of the time delay as the PI filter bandwidth is varied. This is shown in Figure 3(b). The clock jitter increases as the time delay is increased. However, this is most pronounced for the PI filter bandwidth,  $f_{bw}$ , of 3 MHz and 5 MHz. The loop's dynamical behavior becomes more unstable resulting in increased timing jitter as the time delay approaches its critical value, ( $\tau_d^c = 1/2\pi f_{bw}$ ). The impact of time delay on timing jitter is negligible as long as we are far away from the critical value.

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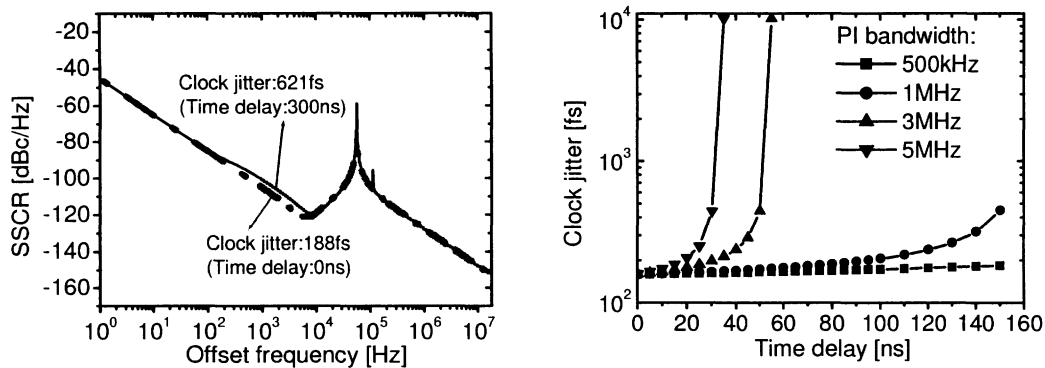


Fig. 3. (a) SSCR of clock signal for zero and 300 ns, respectively. (b) Clock jitter as a function of time delay for selected PI filter bandwidths.

Next, we investigate how the timing jitter of the extracted clock is affected by a time delay as we vary the input data and VCO signal timing jitter (jitter transfer function). In Figure 4, the timing jitter of the extracted clock signal is plotted as a function of input OTDM data signal jitter for selected values of VCO jitter (225 fs, 711 fs and 5 ps). The computations are made for two cases, namely zero and 140 ns time delay. For the relatively large value of VCO jitter (5 ps), a large increase in clock jitter is observed as the time delay is increased from zero to 140 ns. Furthermore, it should be observed that the clock timing jitter is almost constant with respect to input jitter. Timing jitter of the VCO is large and therefore it dominates the clock jitter. Reducing the timing jitter of the VCO reduces the impact of the time delay on the clock jitter as seen in Figure 4. For relatively low VCO timing jitters of 225 fs the impact of time delay on the clock jitter becomes negligible for input signal jitter above approximately 100 fs. Furthermore, reducing the VCO jitter, the extracted clock jitter becomes more dependent on the input OTDM data signal jitter. The clock jitter corresponds approximately to the input OTDM data signal jitter when the VCO jitter is 225 fs and the time delay is zero.

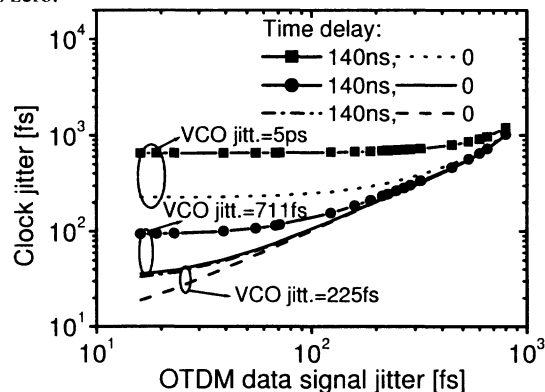


Fig. 4. Jitter transfer function for zero and 140 ns time delay. PI filter bandwidth: 1 MHz.

## 5. Conclusion

We have shown that the minimum clock signal jitter approaches the input data signal jitter when the input data signal jitter and the VCO jitter are relatively low. Increasing the loop length results in an increase in timing jitter as time delay approaches its critical value. The impact of time delay on the clock jitter can be reduced by using a low noise VCO and a low PI filter bandwidth.

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